Electronic Version
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Claims

[c1] 1. A method for fabricating a semiconductor device structure, the method comprising:
forming a silicon germanium (SiGe) layer on a substrate;
forming a silicon layer on the SiGe layer;
forming a gate oxide layer on the silicon layer;
forming a gate structure on the gate oxide layer;
forming a lightly doped drain region in the silicon layer;
forming a spacer on a sidewall of the gate structure;
performing a doping process on the silicon layer to form a heavily doped drain region beside the lightly doped drain region, and on the gate structure;
forming a cap layer over the substrate;
performing an annealing process; and
removing the cap layer.

[c2] 2. The method of claim 1, wherein the doping process is conducted using n-type dopants.

[c3] 3. The method of claim 1, wherein the doping process is conducted using arsenic ions.

[c4] 4. The method of claim 1, wherein a dosage of the doping process is about 3E15 to about 5E15 ions/cm^2.

[c5] 5. The method of claim 1, wherein the doping process is conducted with an implant energy of about 60KeV.

[c6] 6. The method of claim 1, wherein the cap layer is about 300 angstroms to about 700 angstroms thick.

[c7] 7. The method of claim 1, wherein the cap layer comprises a silicon oxide layer.

[c8] 8. The method of claim 1, wherein the annealing process is conducted at about 1000 degrees Celsius for about 10 to 20 seconds.

[c9] 9. The method of claim 1 further comprises forming a silicide layer atop the gate structure and the heavily doped drain region.

[c10] 10. The method of claim 2, wherein the silicide layer is selected from the group consisting of tungsten silicide, titanium silicide, nickel silicide, magnesium silicide, platinum silicide and palladium silicide.

[c11] 11. The method of claim 1, wherein the heavily doped drain region is formed in the silicon layer.

[c12] 12. The method of claim 1, wherein the heavily doped drain region is formed in the silicon layer and the silicon germanium layer.

[c13] 13. The method of claim 1, wherein the heavily doped drain region is formed in the silicon germanium layer.

[c14] 14. The method of claim 1, wherein the gate structure is formed with polysilicon or silicon germanium.

[c15] 15. The method of claim 1, wherein the silicon layer is strained.

[c16] 16. A fabrication method for a semiconductor structure, the method comprising:
providing a silicon substrate;
forming a gate electrode over the silicon substrate;
introducing n-type dopants to the silicon substrate to form source/drain regions in the substrate beside the gate electrode and to the gate electrode;
forming a cap layer the doped polysilicon gate;
performing an annealing process; and
removing the cap layer.

[c17] 17. The method of claim 16, wherein the n-type dopants include arsenic ions.

[c18] 18. The method of claim 16, wherein a dosage of the n-type dopants is about 3E15 ions/cm^2 to about 5E15 ions/cm^2.

[c19] 19. The method of claim 16, wherein the annealing pro-

cess comprises a rapid thermal annealing process conducted at about 1000 degrees Celsius for about 10 to 20 seconds.

[c20] 20. The method of claim 16, wherein the cap layer is about 300 to about 700 angstroms thick.

[c21] 21. The method of claim 16, wherein the cap layer comprises a silicon oxide layer deposited at about 400 degrees to 500 degrees Celsius.

[c22] 22. The method of claim 16, wherein the gate electrode is formed with polysilicon or silicon germanium.

[c23] 23. A fabrication method for a semiconductor device, the method comprising:
forming a silicon germanium (SiGe) layer on a substrate;
forming a silicon layer on the SiGe layer;
forming a gate oxide layer on the silicon layer;
forming a gate structure on the gate oxide layer;
implanting arsenic ions to the strained silicon layer to form a lightly doped drain region;
forming a spacer on a sidewall of the gate;
implanting arsenic ions to the strained silicon layer and a top surface of the silicon germanium layer to form a heavily doped drain region beside the lightly doped drain region and to the gate structure;

forming a cap layer over the substrate;

performing a rapid thermal annealing process;

removing the cap layer;

forming a nickel silicide layer atop the gate structure and the heavily doped drain region.

[c24] 24. The method of claim 23, wherein the gate structure is formed with polysilicon or silicon germanium.

[c25] 25. The method of claim 23, wherein a dosage used implanting the arsenic ions to the strained silicon layer and a top surface of the silicon germanium layer, and to the gate structure is about 3E15 to about 5E15 ions/cm^2.